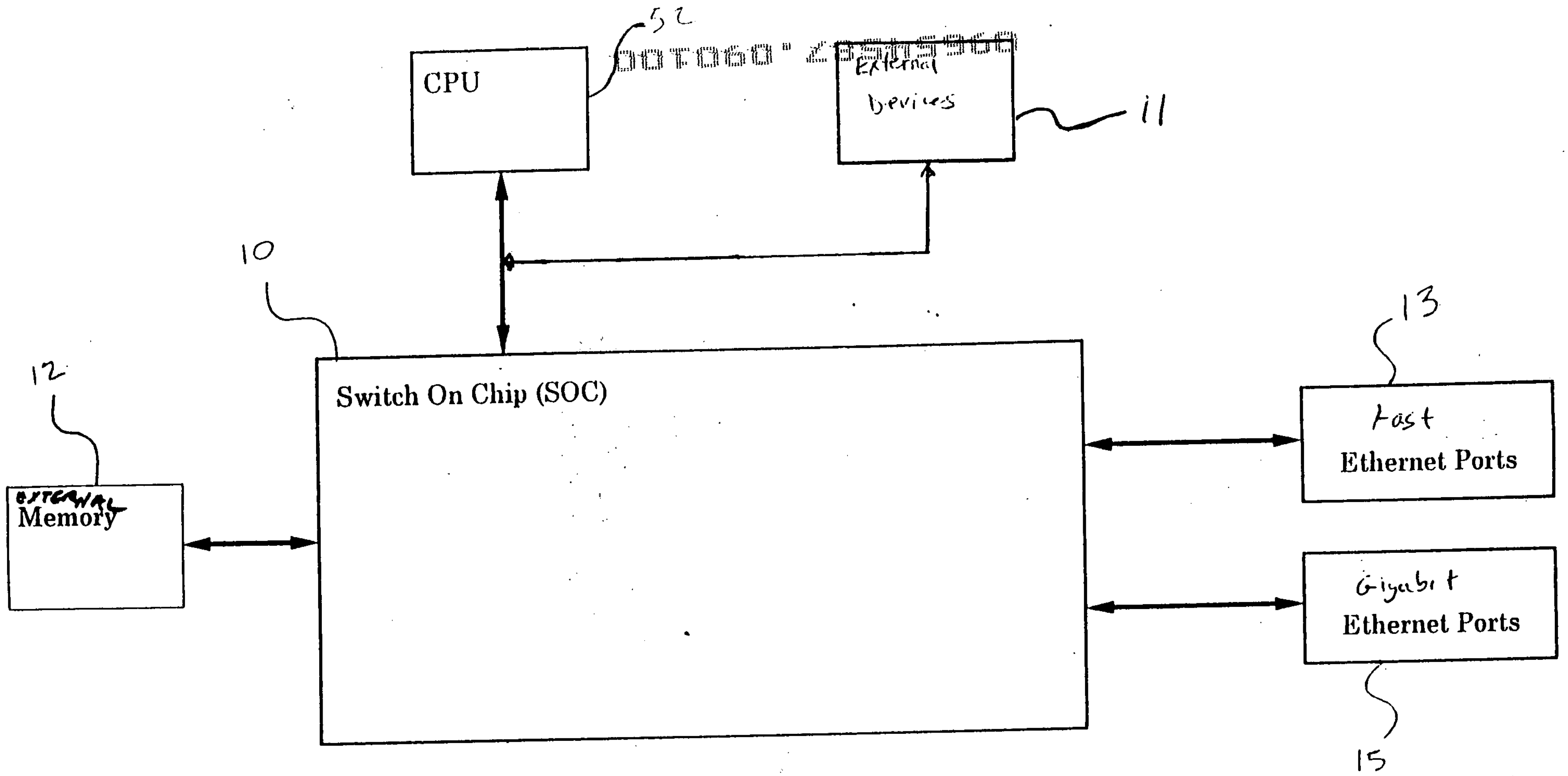
CPU
52
External Devices
11
10
Switch On Chip (SOC)
12
External Memory
13
Fast Ethernet Ports
Gigabit Ethernet Ports
15

Fig. 1

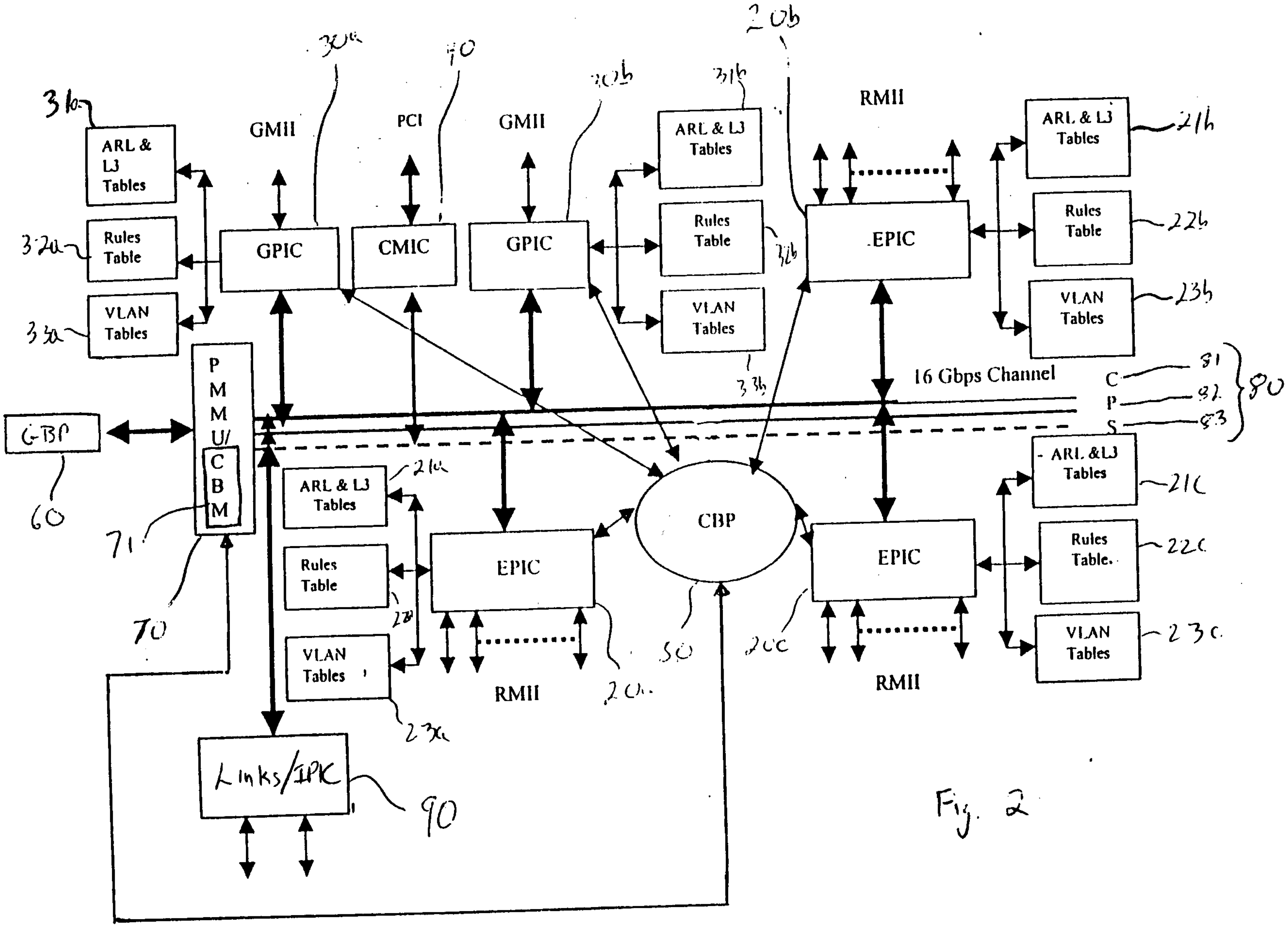
GMII
PCI
GMII
RMII
30a
10
20b
31b
20b
31a
ARL & L3 Tables
32a
Rules Table
33a
VLAN Tables
GPIC
CMIC
GPIC
ARL & L3 Tables
Rules Table
32b
VLAN Tables
33b
EPIC
ARL & L3 Tables
21b
Rules Table
22b
VLAN Tables
23b
16 Gbps Channel
C
P
S
81
82
83
80
GBP
60
P
M
M
U/
C
B
M
71
70
ARL & L3 Tables
21a
Rules Table
22a
VLAN Tables
23a
EPIC
RMII
20a
CBP
50
EPIC
20c
RMII
ARL & L3 Tables
21c
Rules Table
22c
VLAN Tables
23c
Links/IPC
90

Fig. 2

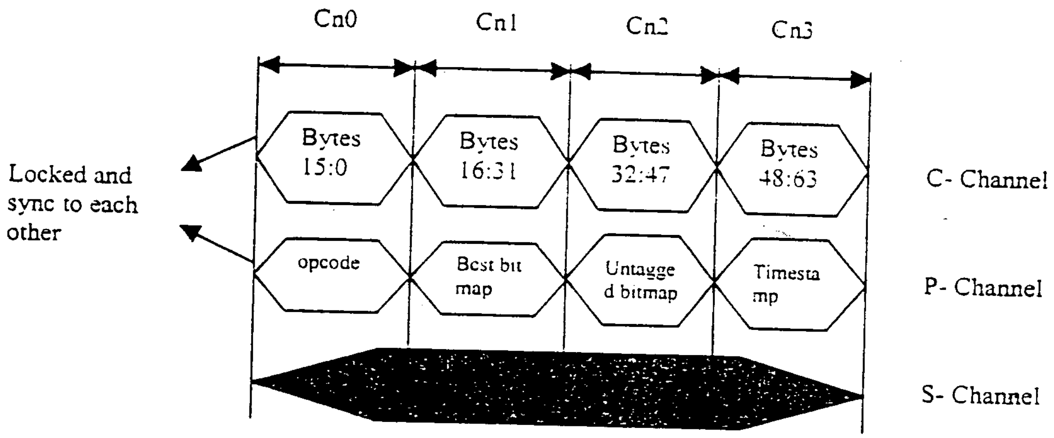
Cn0
Cn1
Cn2
Cn3
Bytes 15:0
Bytes 16:31
Bytes 32:47
Bytes 48:63
C- Channel
opcode
Best bit map
Untagged bitmap
Timestamp
P- Channel
S- Channel
Locked and sync to each other

Fig. 3

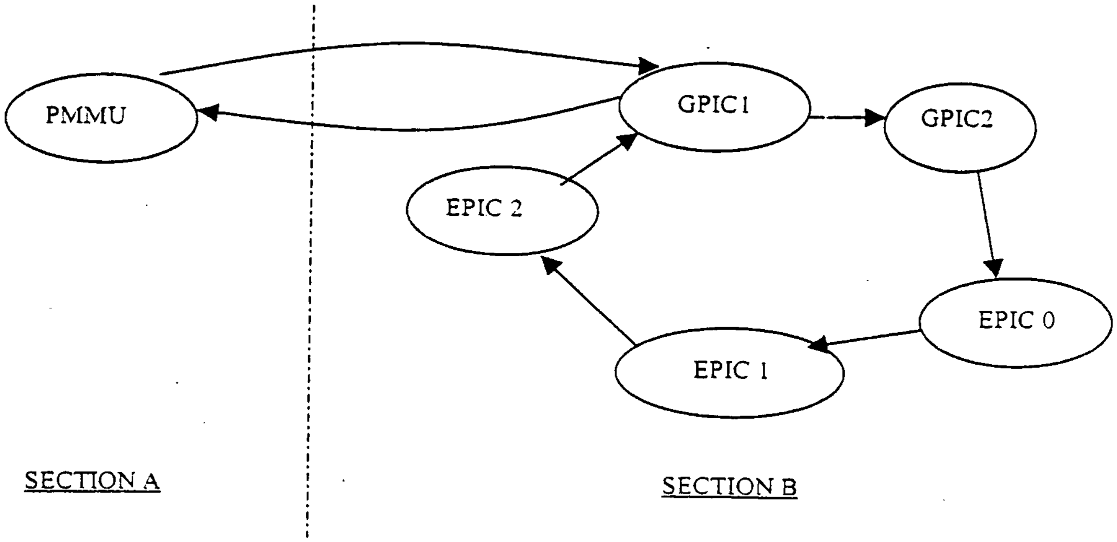
PMMU
GPIC1
GPIC2
EPIC 2
EPIC 0
EPIC 1
SECTION A
SECTION B

Fig. 4a

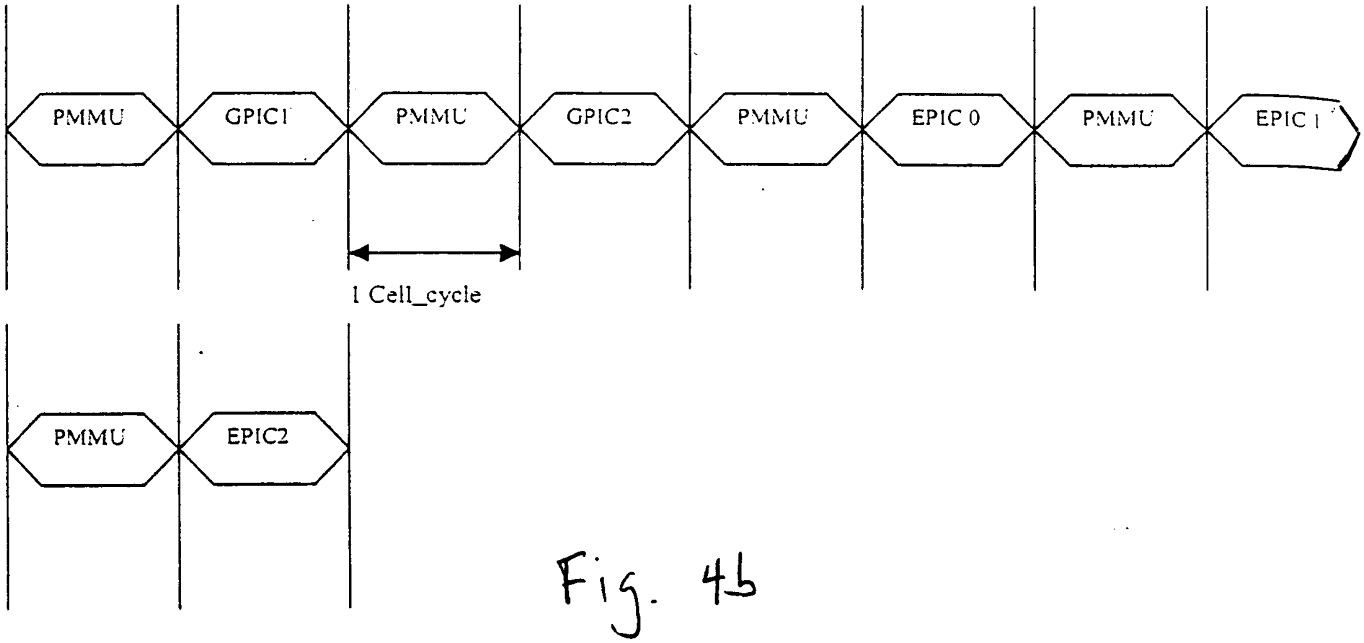
PMMU
GPIC1
PMMU
GPIC2
PMMU
EPIC 0
PMMU
EPIC 1
1 Cell_cycle
PMMU
EPIC2

Fig. 4b

Protocol Channel Messages

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
Opcode	Ip IPX	Reserved	Nxt cell	Src Dest Port			Cos	J	S E	Crc	P O	Len			

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
Reserved		Bc/Mc Portbitmap													

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
U	Res	Untagged Portbitmap / Src Port Number (bit0..5)													

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
CPU Opcodes									TimeStamp						

Fig. 5

Side Band Channel Messages

30 28 26	24 22 20	18 16 14	12 10 8	6	4	2	0
Opcode	Dest Port / Destination Dev Id	Src Port	DataLen	E	EC ode	Cos	C
Address							
Data							

Fig. 6

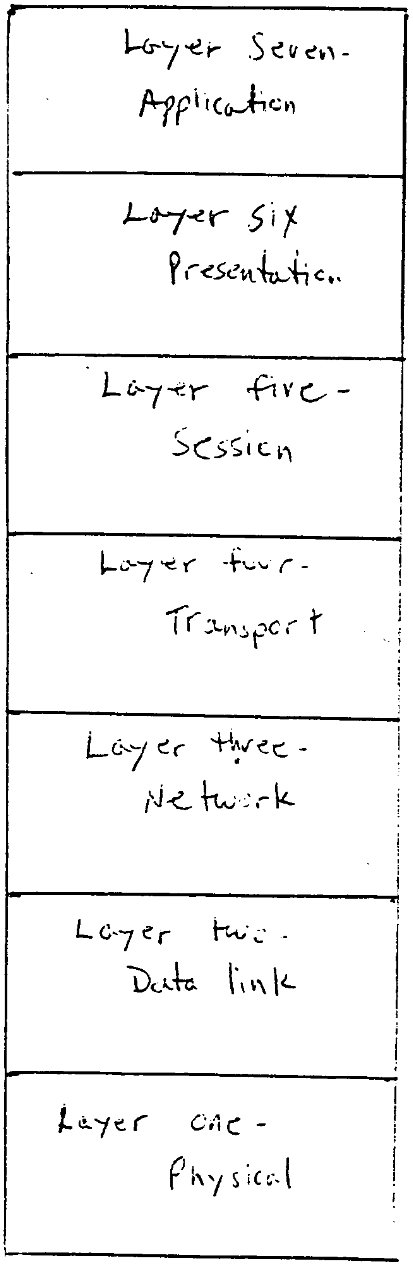

Figure 7
Prior Art

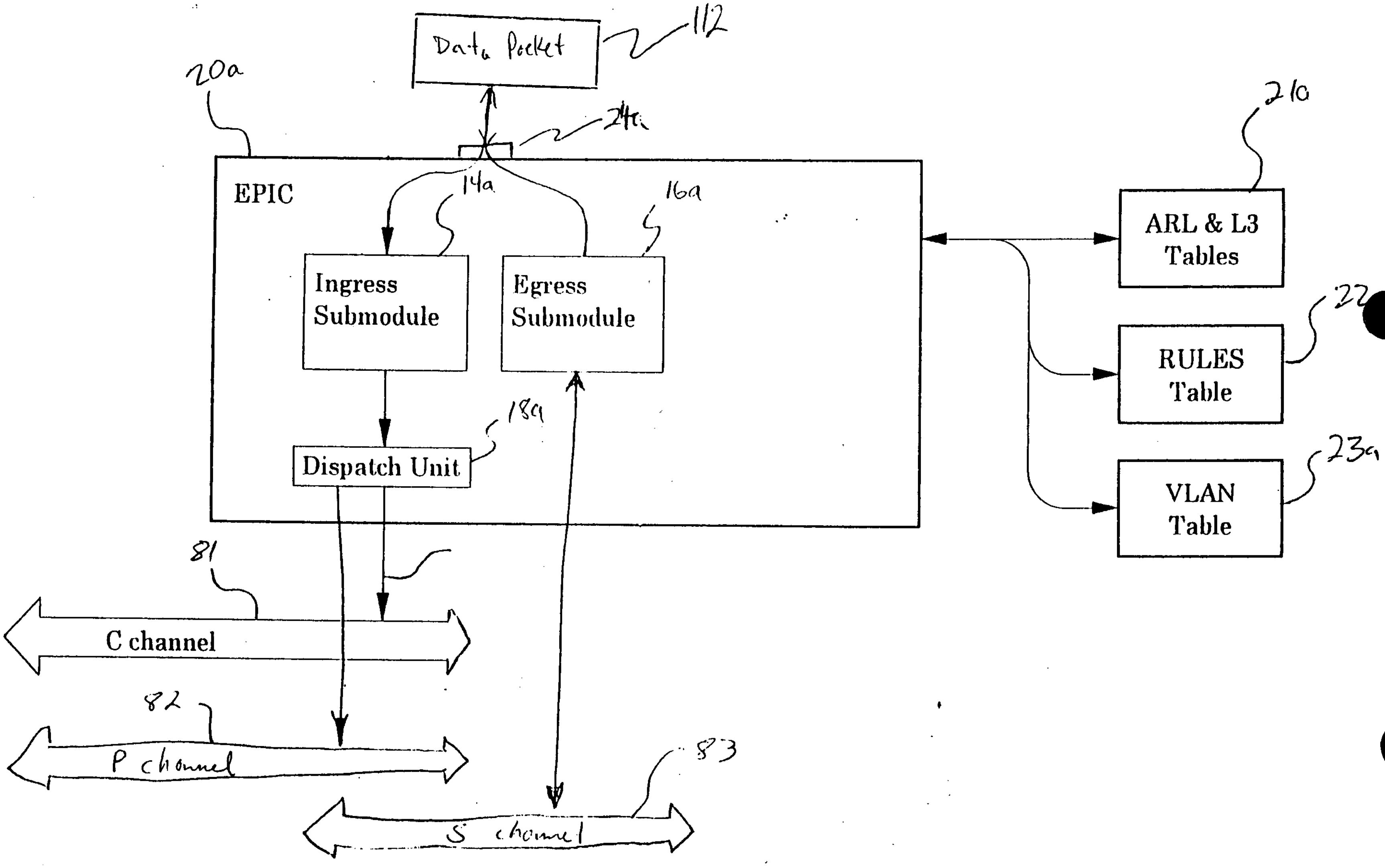
Data Packet
112
20a
24a
EPIC
14a
16a
Ingress Submodule
Egress Submodule
18a
Dispatch Unit
21a
ARL & L3 Tables
22a
RULES Table
23a
VLAN Table
81
C channel
82
P channel
83
S channel

Fig 8

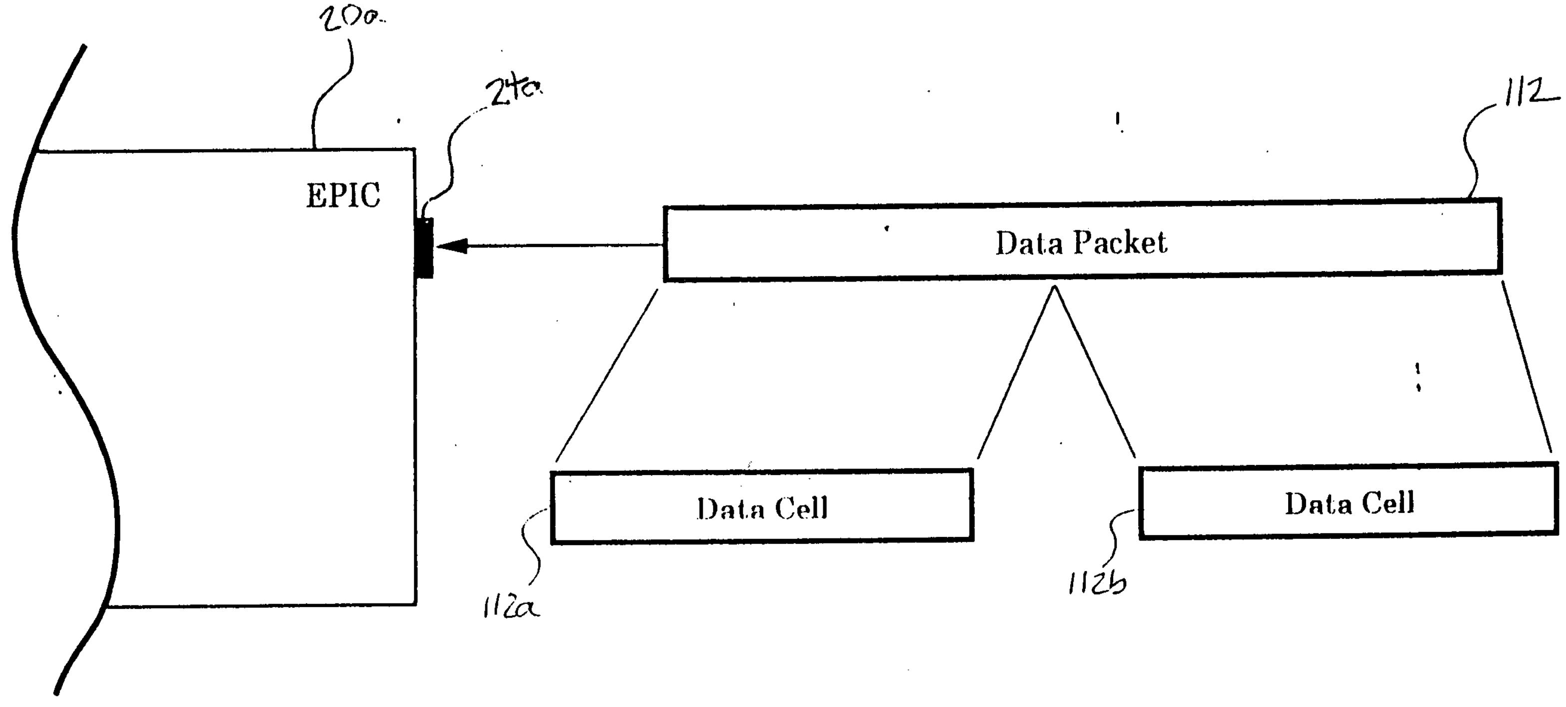

Fig. 9

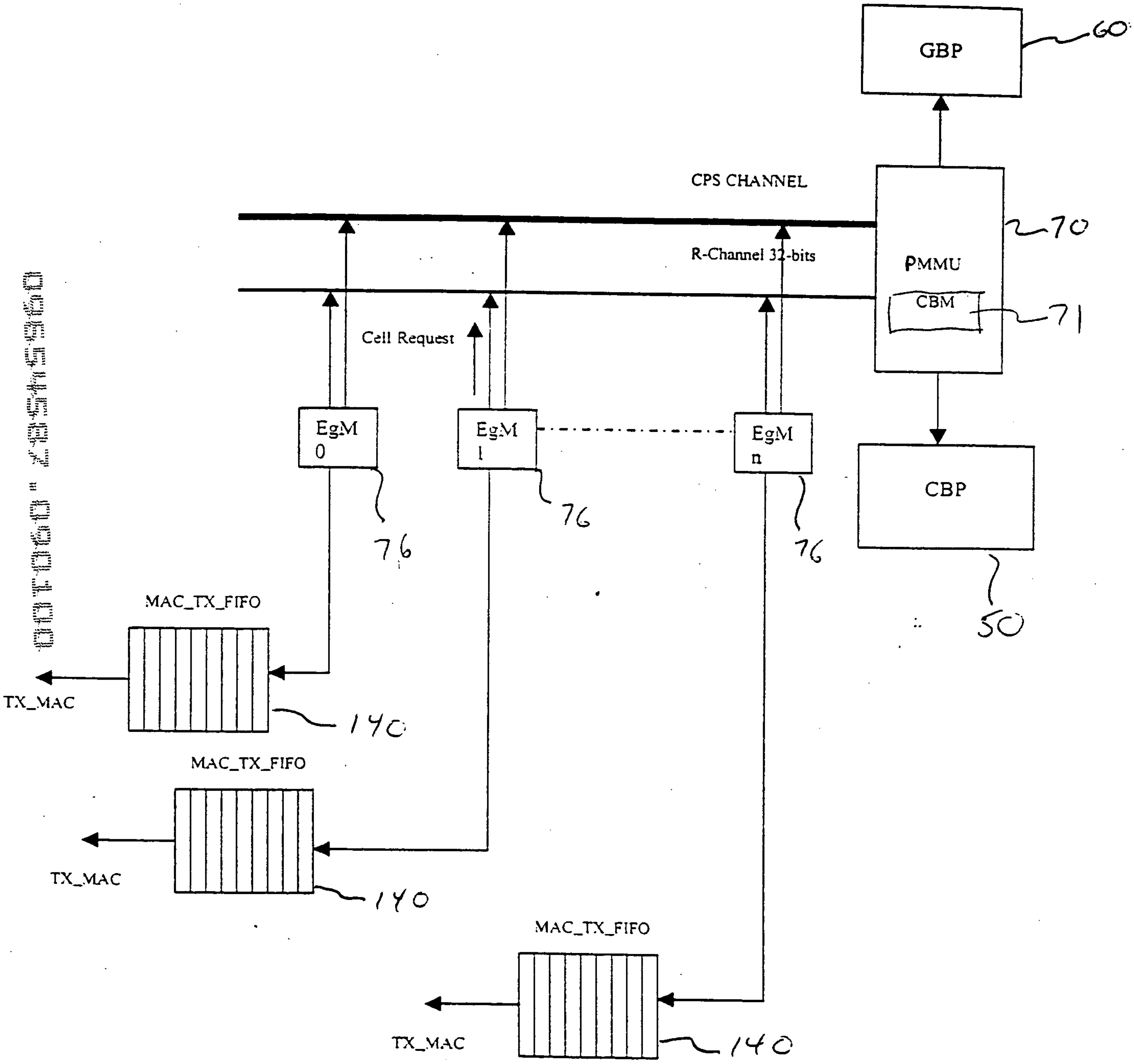
GBP
60
CPS CHANNEL
70
PMMU
CBM
71
R-Channel 32-bits
Cell Request
EgM 0
EgM 1
EgM n
76
76
76
CBP
50
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140

Fig. 10

<table>
<tr><td>Line 0 →</td><td>FC ¦ LC ¦ BC/MC ¦ Cpy_cnt(5b) ¦ Cell_length (7b) . CRC (2b) ¦ NC_header (16b) Src Count(6)¦IPX/IP ¦Time_Stamp (14b) ¦ O bits(2b) ¦ P¦ NextCellLen(2b)¦CpuOpcode(4b)¦ Cell_data (0-9B)</td></tr>
<tr><td>Line 1 →</td><td>Cell_data (10-27) Bytes</td></tr>
<tr><td>Line 2 →</td><td>Cell_data (28-45) Bytes</td></tr>
<tr><td>Line 3 →</td><td>Cell_data (46-63) Bytes</td></tr>
</table>

Fig. 11

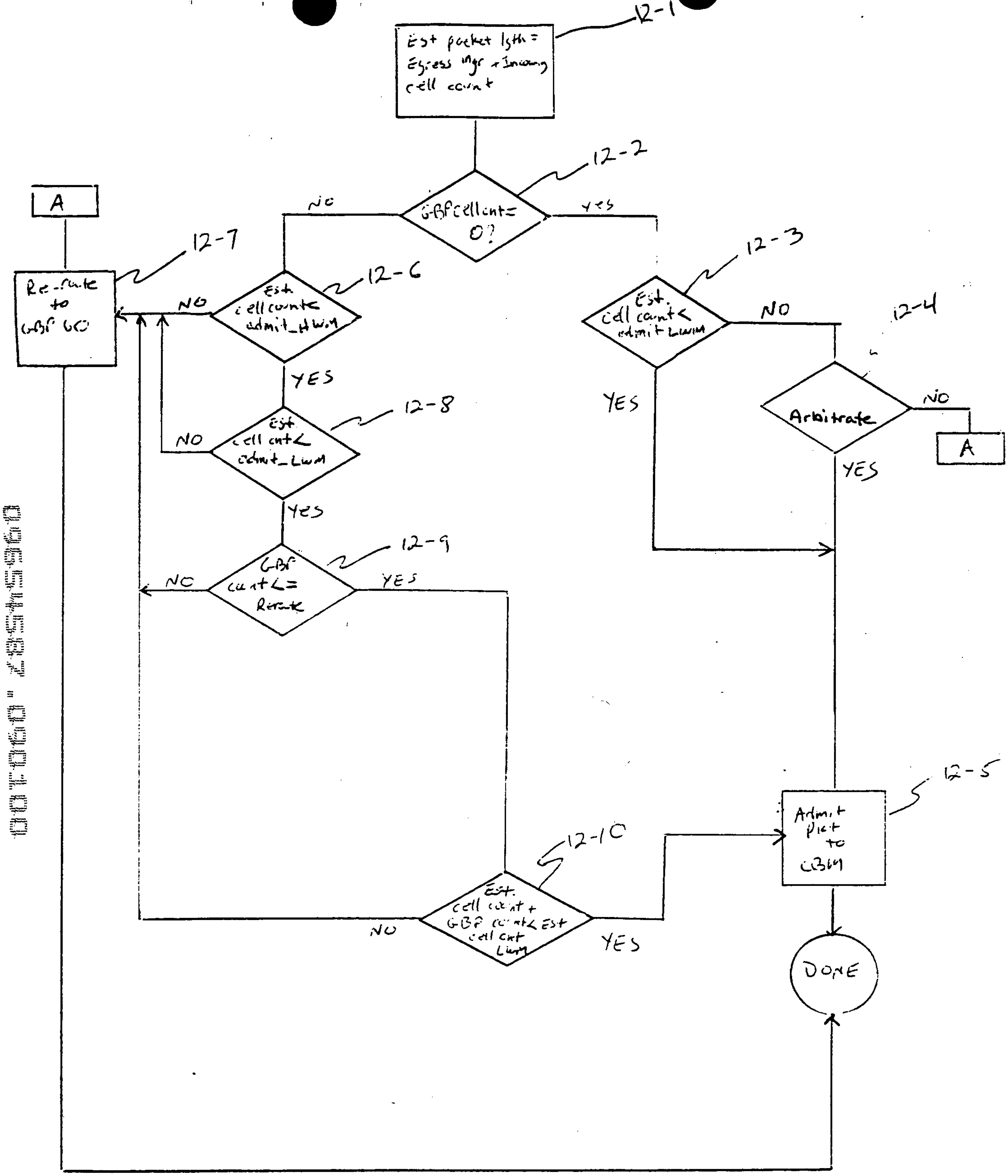
12-1
Est packet lgth = Egress Mgr + Incoming cell count
12-2
GBF cell cnt = 0?
NO
YES
A
12-7
Re-route to GBF GO
12-6
Est cell count < admit_HWM
NO
YES
12-3
Est. cell count < admit LWM
NO
YES
12-4
Arbitrate
NO
A
YES
12-8
Est cell cnt < admit_LWM
NO
YES
12-9
GBF cnt <= Reroute
NO
YES
12-5
Admit Pkt to CBM
12-10
Est. cell count + GBF count < Est cell cnt LWM
NO
YES
DONE

Fig. 12

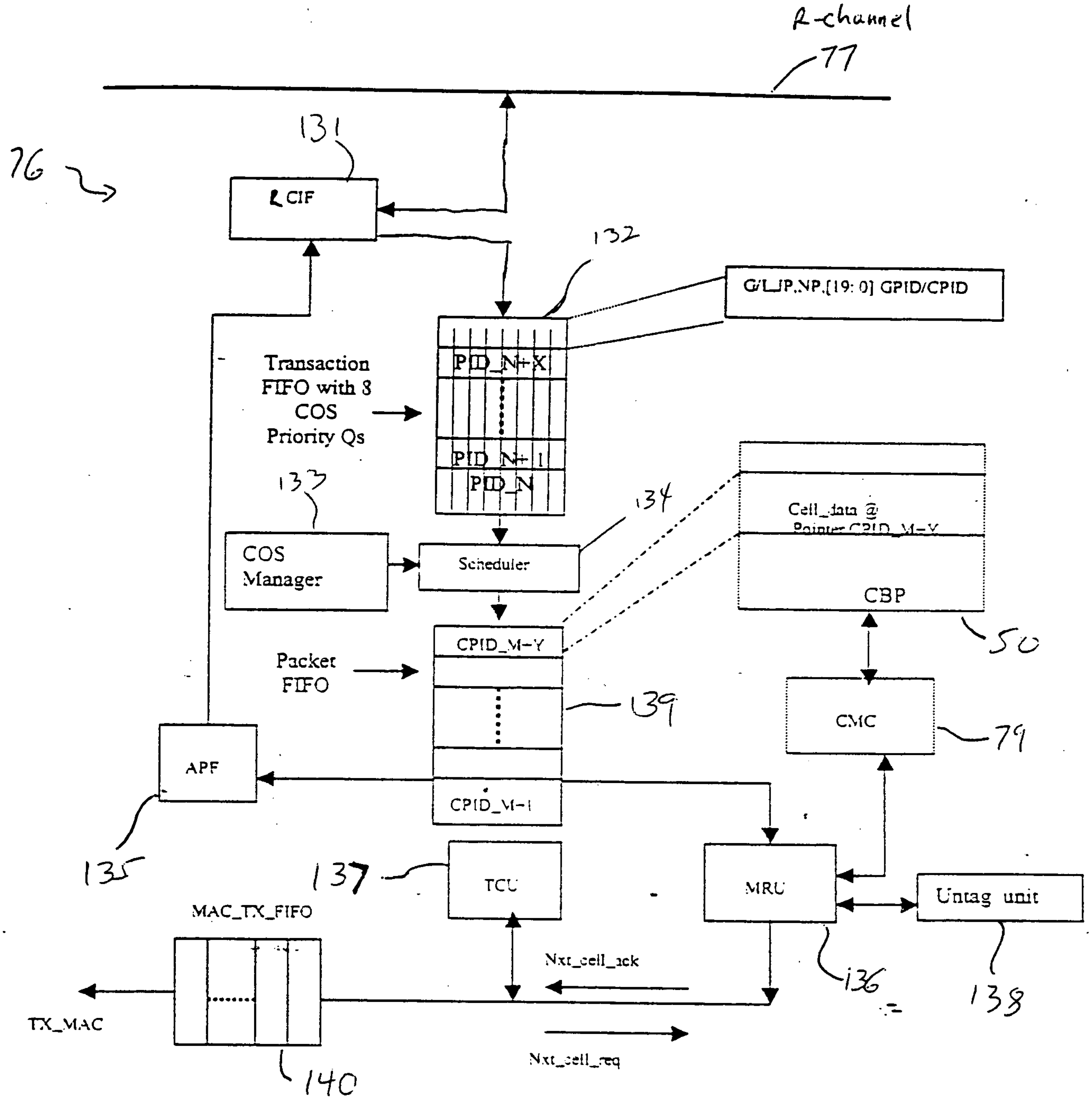
R-channel
77
131
76
R CIF
132
G/L,IP,NP,[19:0] GPID/CPID
PID_N+X
Transaction FIFO with 8 COS Priority Qs
PID_N+1
PID_N
133
134
Cell_data @ Pointer CPID_M-Y
CBP
COS Manager
Scheduler
50
CPID_M-Y
Packet FIFO
139
CMC
79
APF
CPID_M-1
135
137
TCU
MRU
Untag unit
MAC_TX_FIFO
Nxt_cell_ack
TX_MAC
136
138
Nxt_cell_req
140

Fig 13

Data Flow

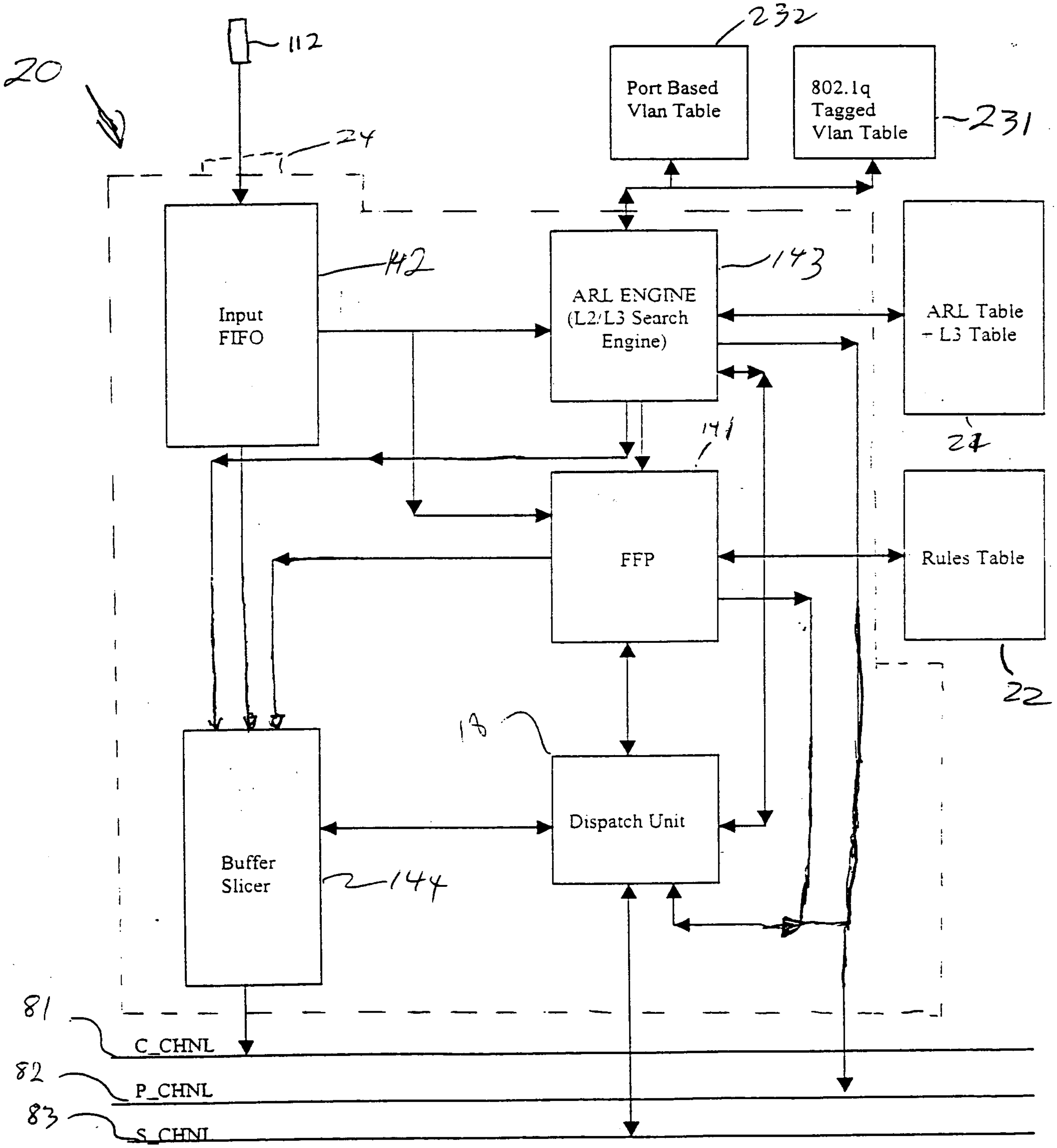

Fig. 14

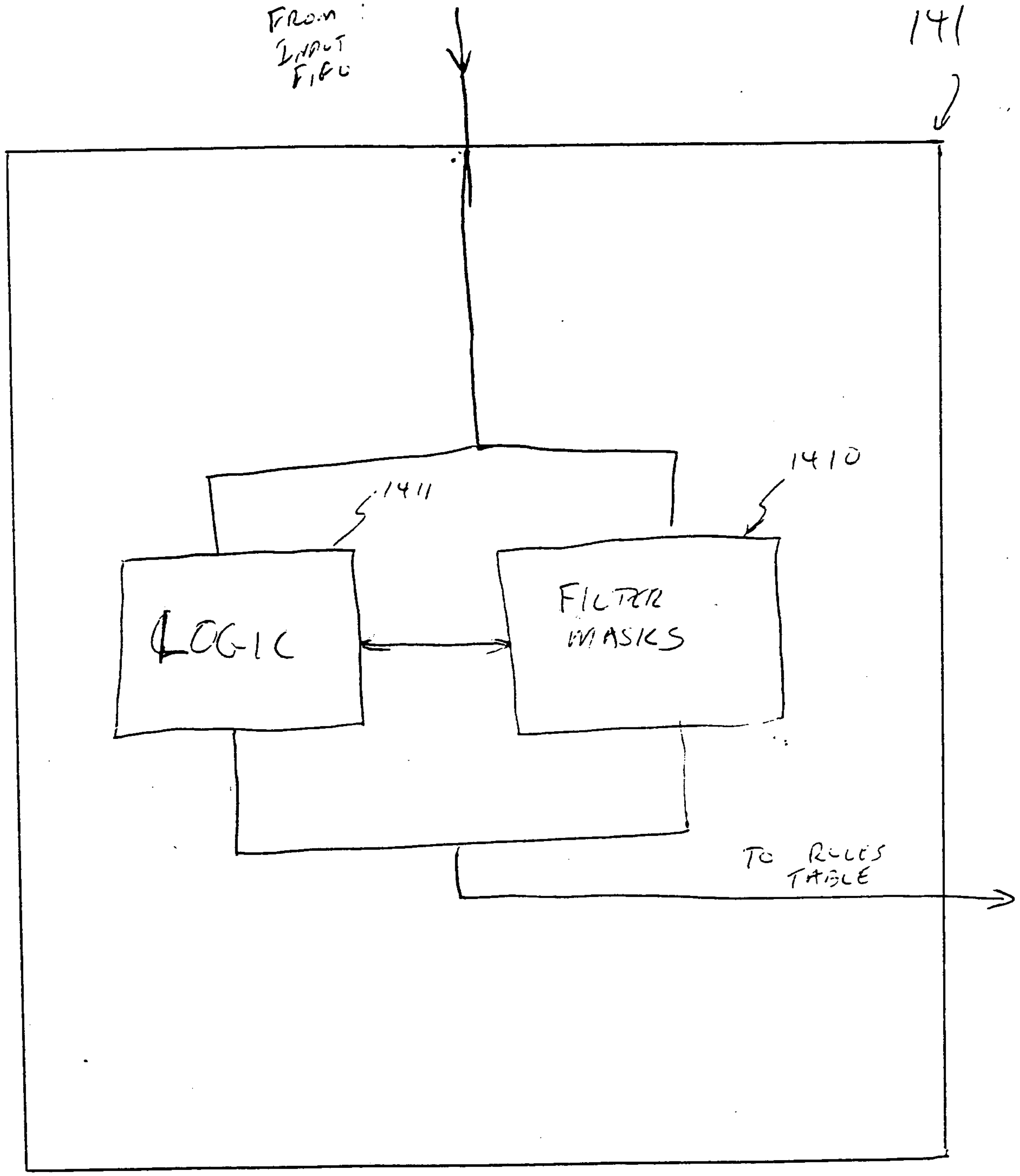
FROM INPUT FIFO
141
1411
1410
LOGIC
FILTER MASKS
TO RULES TABLE

FIG. 15

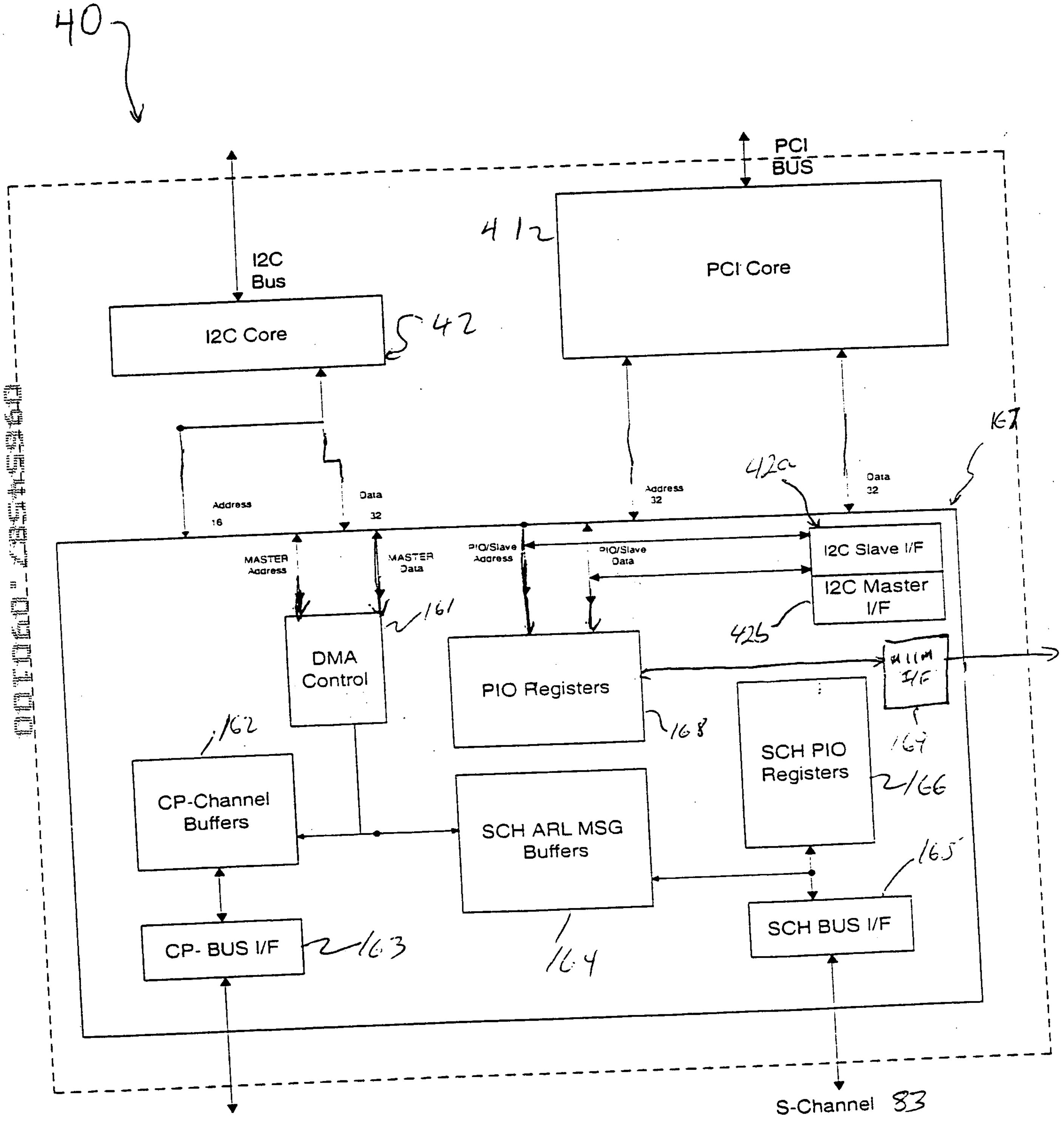
40
I2C Bus
PCI BUS
412
PCI Core
I2C Core
42
Address 16
Data 32
Address 32
Data 32
42a
167
MASTER Address
MASTER Data
PIO/Slave Address
PIO/Slave Data
I2C Slave I/F
I2C Master I/F
42b
161
DMA Control
PIO Registers
168
HIM I/F
169
162
CP-Channel Buffers
SCH ARL MSG Buffers
SCH PIO Registers
166
165
SCH BUS I/F
CP- BUS I/F
163
164
S-Channel 83
C channel 81
P channel 82

Fig. 16

FFP Programming Flow Chart

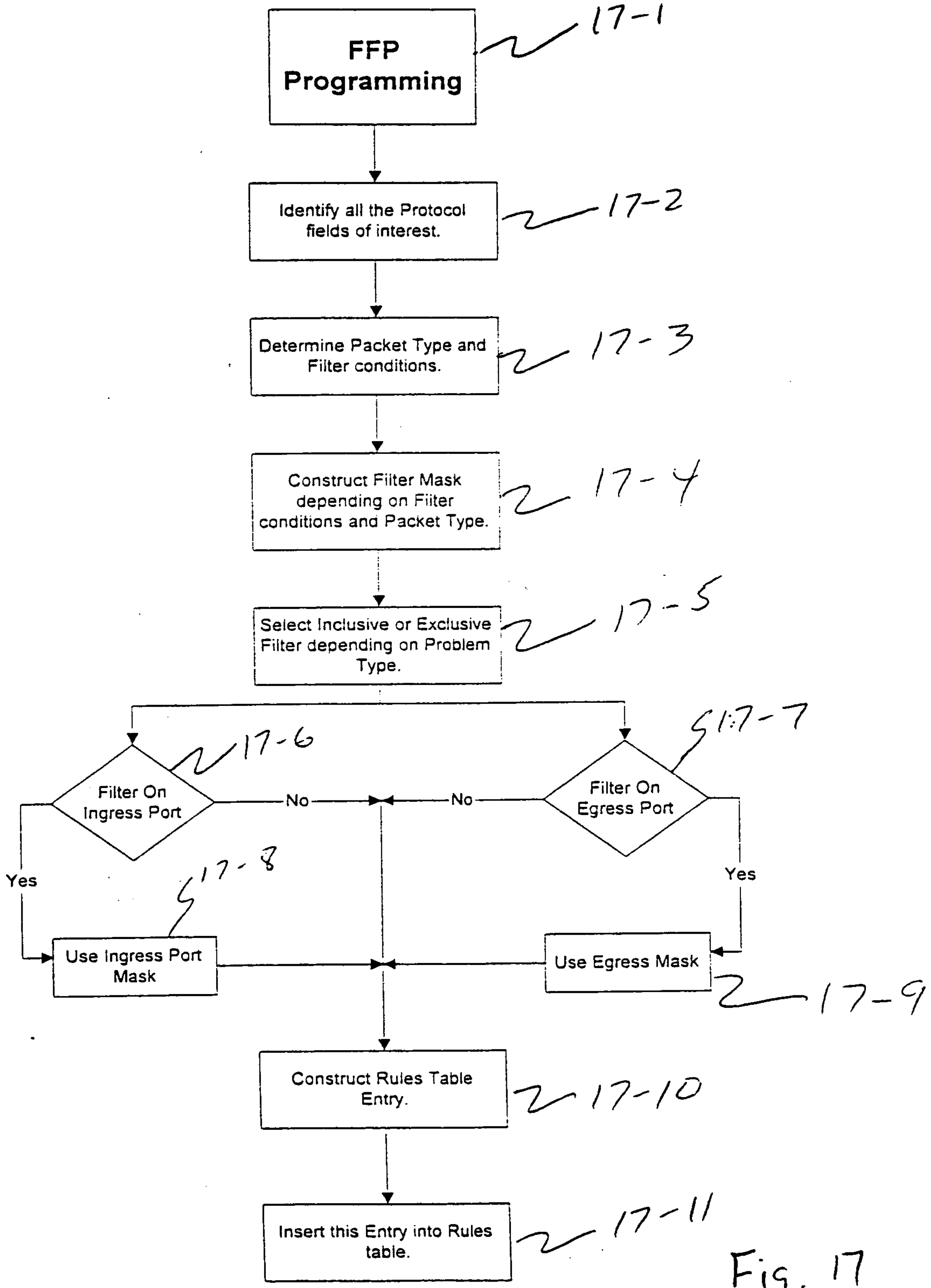

Fig. 17

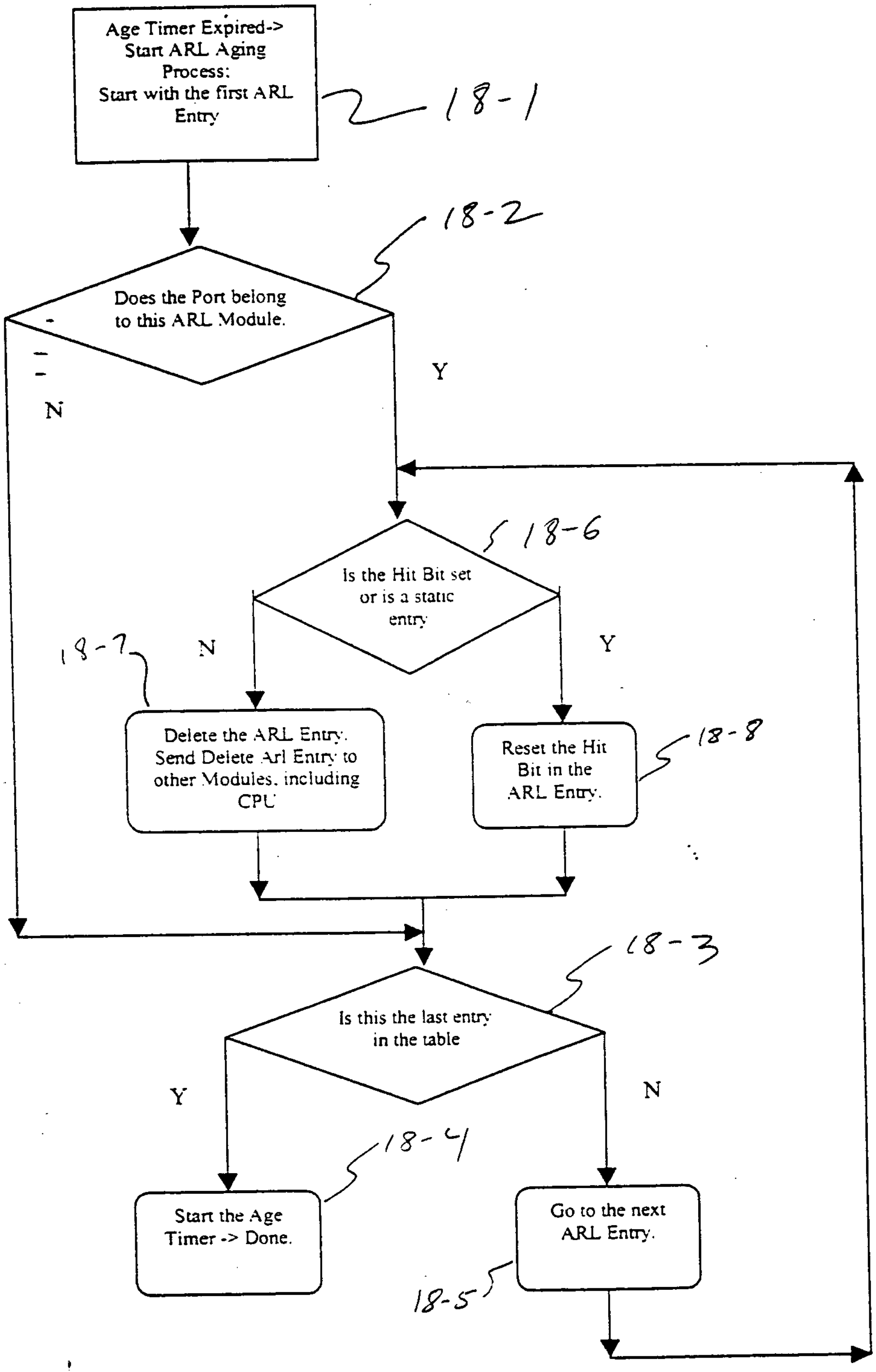
Age Timer Expired-> Start ARL Aging Process: Start with the first ARL Entry
18-1
18-2
Does the Port belong to this ARL Module.
Y
N
18-6
Is the Hit Bit set or is a static entry
N
Y
18-7
Delete the ARL Entry. Send Delete Arl Entry to other Modules, including CPU
Reset the Hit Bit in the ARL Entry.
18-8
18-3
Is this the last entry in the table
Y
N
18-4
Start the Age Timer -> Done.
Go to the next ARL Entry.
18-5

Fig. 18

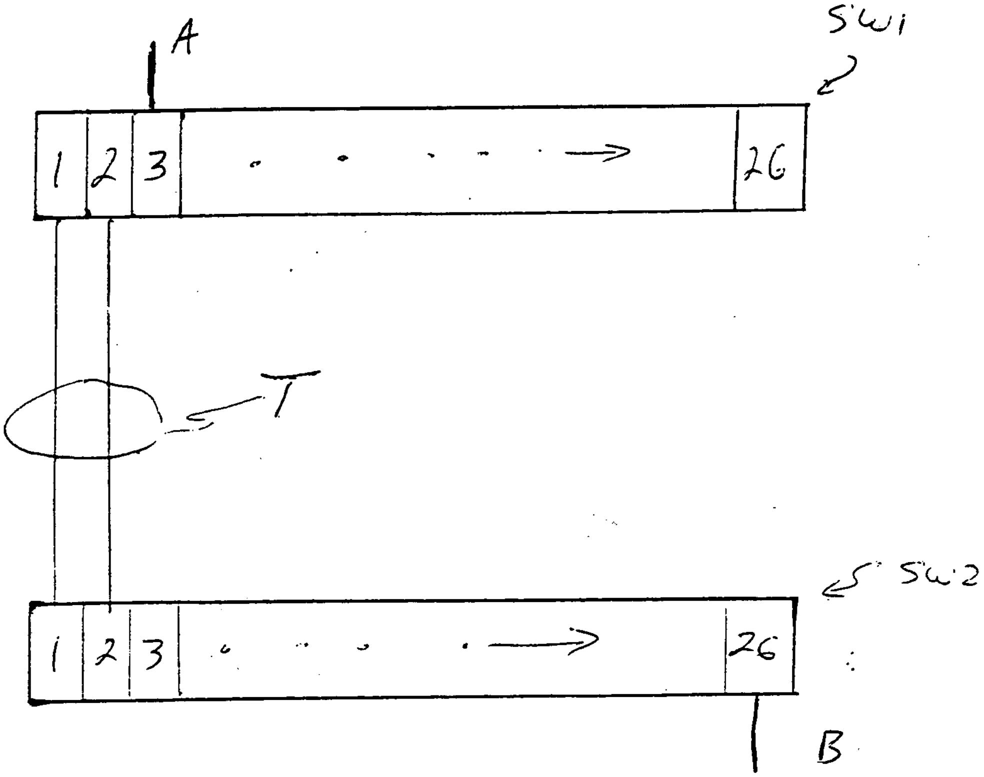

Fig. 19

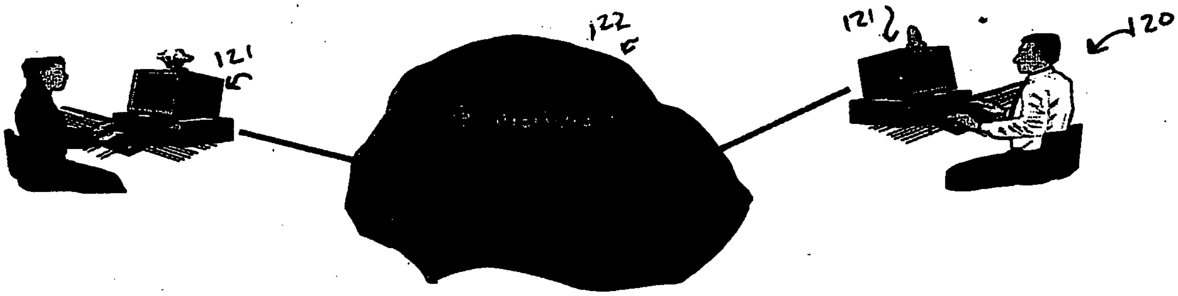

FIGURE 20

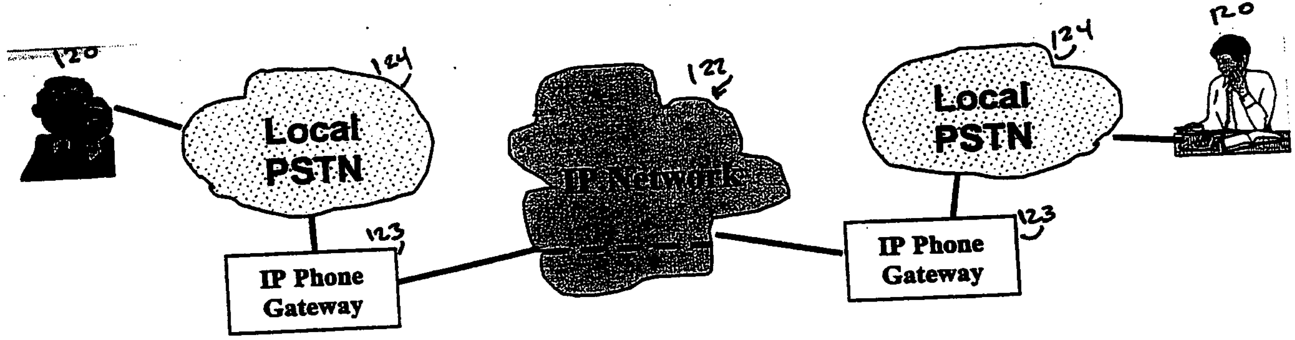
120
124
Local PSTN
122
IP Network
123
IP Phone Gateway
124
Local PSTN
120
123
IP Phone Gateway

FIGURE 21

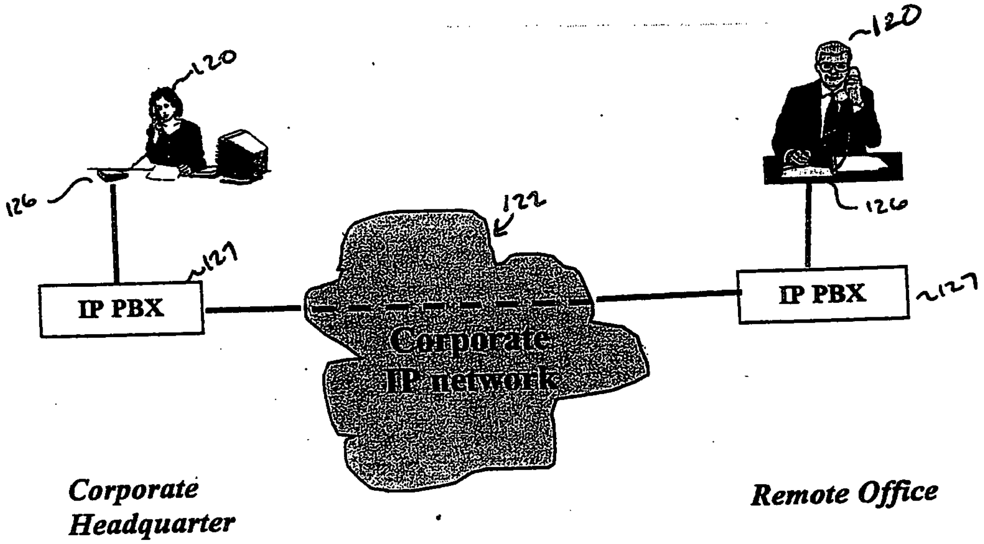

FIGURE 22

Figure 4: IP-PBX Used in Enterprise

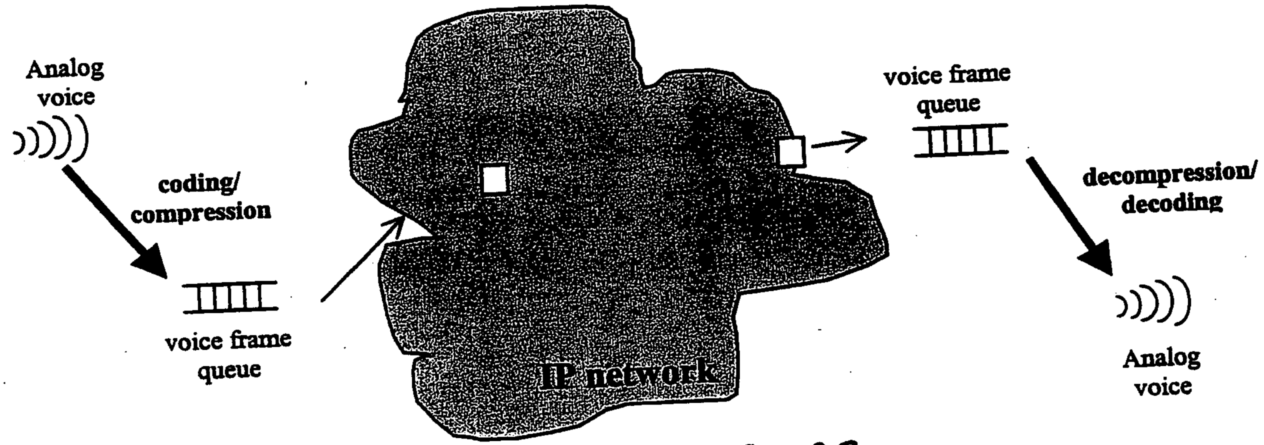
Analog voice
coding/ compression
voice frame queue
IP network
voice frame queue
decompression/ decoding
Analog voice

FIGURE 23

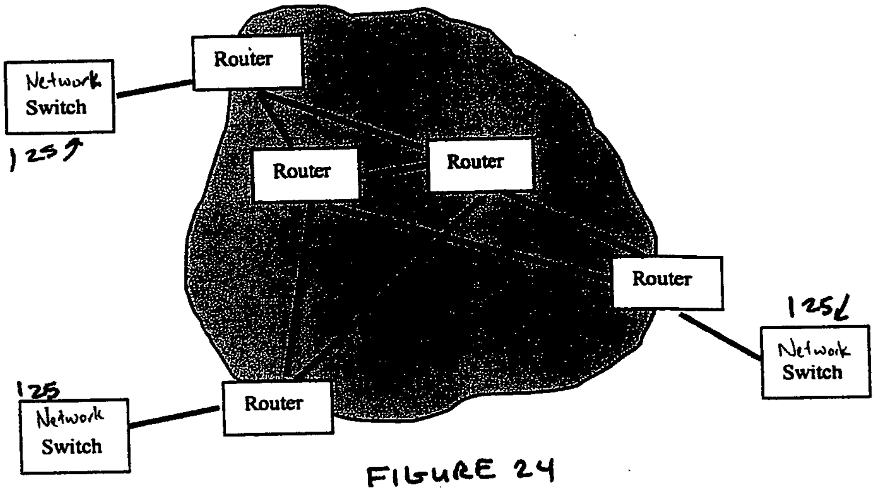
Network Switch
Router
125
Router
Router
Router
125
Network Switch
125
Network Switch
Router

FIGURE 24

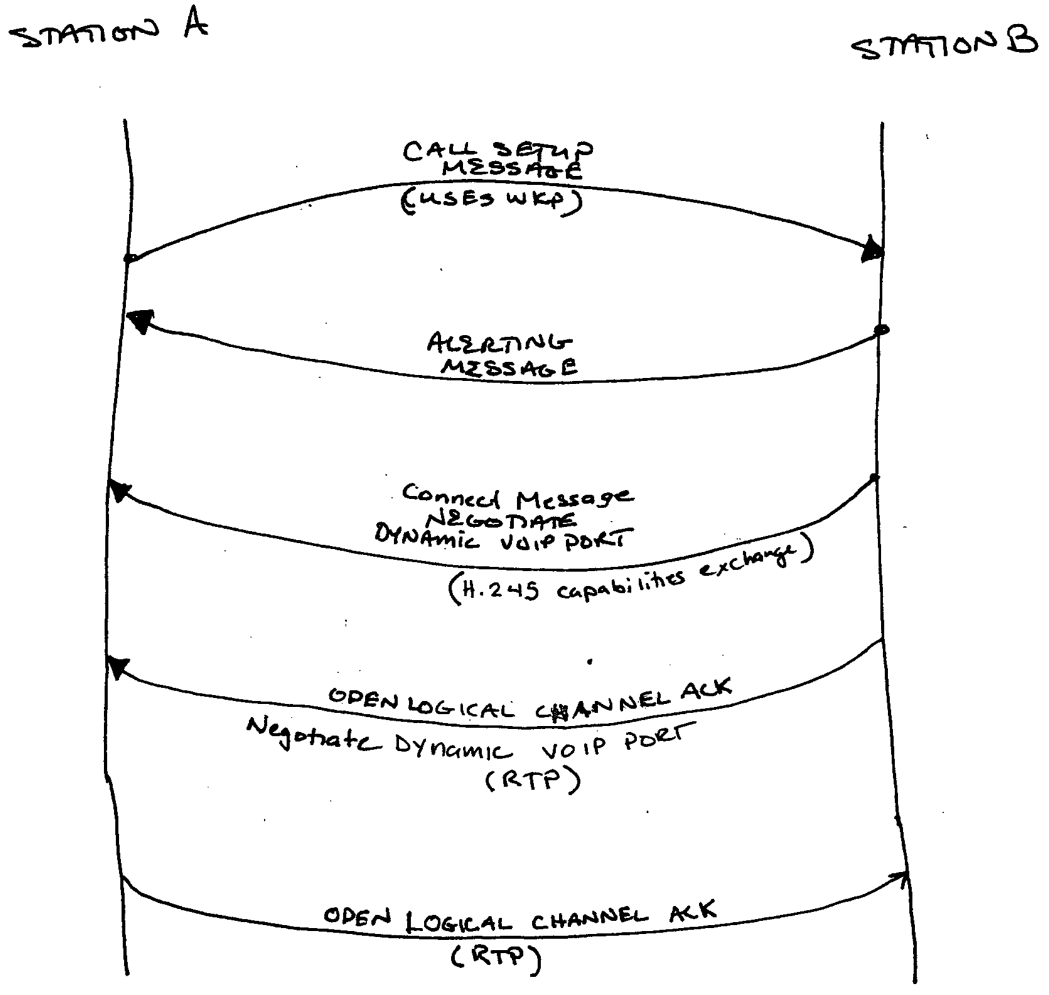
STATION A
STATION B
CALL SETUP MESSAGE
(USES WKP)
ALERTING MESSAGE
Connect Message
NEGOTIATE DYNAMIC VOIP PORT
(H.245 capabilities exchange)
OPEN LOGICAL CHANNEL ACK
Negotiate Dynamic VOIP PORT
(RTP)
OPEN LOGICAL CHANNEL ACK
(RTP)

FIGURE 25

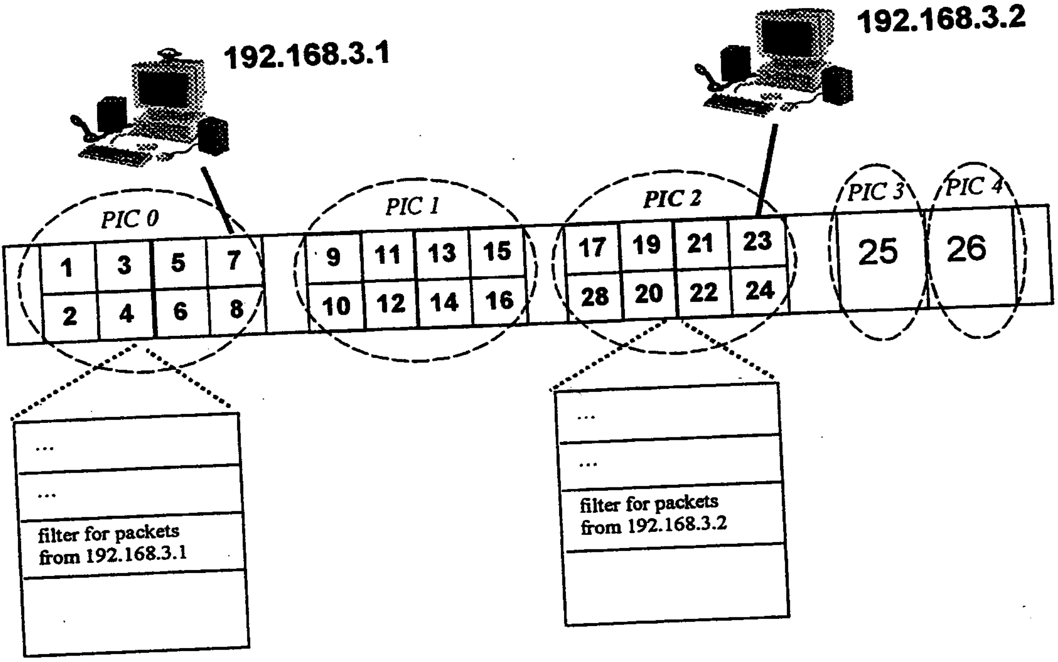
192.168.3.1
192.168.3.2
PIC 0
PIC 1
PIC 2
PIC 3
PIC 4
1
3
5
7
2
4
6
8
9
11
13
15
10
12
14
16
17
19
21
23
28
20
22
24
25
26
...
...
filter for packets from 192.168.3.1
...
...
filter for packets from 192.168.3.2

FIGURE 26

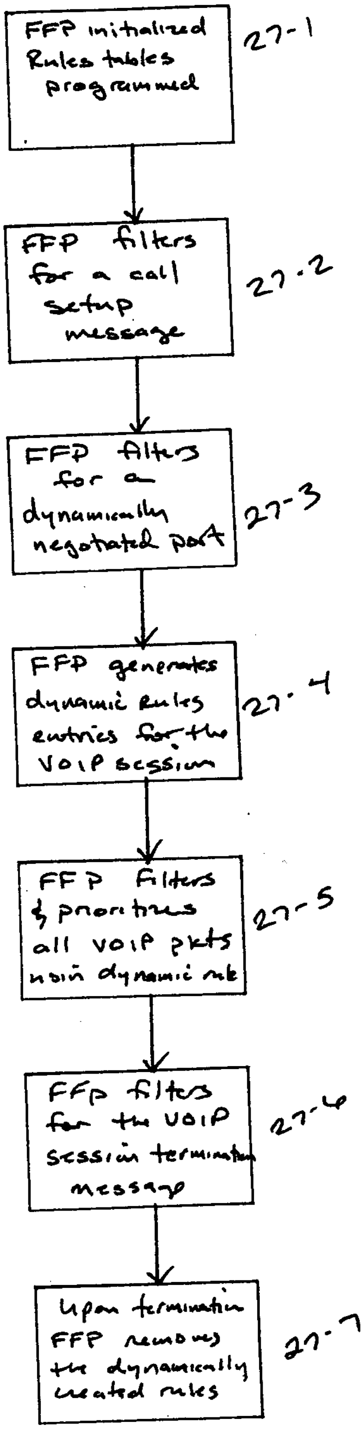
FFP initialized Rules tables programmed
27-1
FFP filters for a call setup message
27-2
FFP filters for a dynamically negotiated port
27-3
FFP generates dynamic Rules entries for the VOIP session
27-4
FFP Filters & prioritizes all VOIP pkts usin dynamic rule
27-5
FFp filters for the VOIP session termination message
27-6
Upon termination FFP removes the dynamically created rules
27-7

FIGURE 27